CENTAR

Datasheet: Fixed-Size FFT

Features

- ***High Throughput***: obtained from high clock rates (>500MHz using 65nm technology) and novel algorithms
- ***FFT size***: User chosen power-of-two or non-power-of-two
- ***Programmability***: Finite-state-machine control circuitry for matching circuit/application functionality and I/O interface.
- ***Dynamic Range***: combined block floating point and floating point architecture means smaller word lengths can be used for post-processing operations such as equalization (~6db/bit).
- ***Scalability***: array based architecture means arbitrarily higher throughputs are obtained by increasing array size
- ***Power***: array interconnects are entirely local, reducing parasitic routing capacitance to keep power dissipation low and clock speeds high
- ***Implementation FPGA***: Centar's DFT circuit can be used in any FPGA fabric containing embedded multipliers and memories.
- ***Data I/O*****:** Streaming, normal order I/O with fixed-point 2's complement input words

Options

- Fixed point word input lengths (2's complement)
- Output format
  - Fixed-point
  - Block floating-point
  - Floating-point

Algorithm

The transform computation is based on a new formulation[1] of the discreet Fourier transform (DFT), different than any other FFT implementation, which decomposes it into structured sets of small, matrix-based DFTs. In particular the locality, simplicity and regularity of the processing core keeps interconnect delays lower than cell delays, leading to clock speeds that can approach the FPGA fabric limitations, e.g., "worst case" Fmax speeds >500MHz in 65nm FPGA technology. Short critical-path lengths with less delay in cells than interconnects also lower power dissipation. Additionally, a novel "base-4" algorithm reduces the number of cycles needed per FFT to less than the transform size value *N*. Finally, it includes a low overhead hybrid floating-point feature that increases dynamic range for a given fixed-point word size.

Architecture

The architecture consists of two small arrays of pipelined, fine-grained, locally connected, simple processing elements, each containing a complex adder, a few registers and multiplexors. By cycling data through this array in a programmable way any size transform can be supported as well as desired variations from the standard DFT calculation.

[1] J. Greg Nash, "Computationally Efficient Systolic Array for Computing the Discreet Fourier Transform, IEEE Trans. Signal Processing, Vol. 53, No.12, December 2005, pp.4640-4641.

Scaling

Word growth during computation is handled automatically using a combination of block floating point (BFP) and floating point (FP) features that provide a much higher dynamic range than other fixed-point FFT circuits with the same input word length. A measure of dynamic range in in decibels is the ratio of the magnitude of the sum of the two large FFT coefficients and the largest round-off noise value for "single tone" real inputs (random frequency and phase):

	Fixed-Size Transform Size Examples				
	128	256	512	1024	2048
Mean	103	105	103	104	105
Std. Dev.	2.7	2.3	4.2	2.2	2.0
Maximum	117	111	115	111	111
Minimum	92	95	96	96	99

Dynamic Range (db) (2000 FFT blocks)

Typically, circuits show almost 6db/bit of dynamic range as defined above.

Signal-to-Quantization-Noise-Ratio (SQNR)

Unlike traditional pipelined FFTs, all additions are performed at full precision so that the round-off errors occur only in the twiddle multiplication multiplication steps. Consequently, the SQNR is much higher than found in other FFT architectures for a given input bit length.

	Fixed-Size Transform Size Examples				
	128	256	512	1024	2048
Mean	87	87	82	83	81
Std. Dev.	1.6	1.4	0.83	0.84	0.62
Maximum	91	90	85	85	83
Minimum	83	83	79	80	79

SQNR (db) (2000 FFT blocks)

Performance and Resources

Here performance and resource usage data is provided on a 256 and 1024-point, streaming variable FFT examples. The circuit was compiled using Intel's software tools (Quartus II) and a Stratix III EP3SE50F484C2 FPGA. The TimeQuest static timing analyzer was used to determine maximum clock frequencies (Fmax) at 1.1V and 85C (worst case settings).

	Intel	Centar v1	Centar v2	Intel	Centar
	20 bits	**16 bits**	**16 bits**	**20 bits**	**16 bits**
Transform Size	256pts			1024pts	
ALMs	4414	4024	5063	4770	4357
Memory (Kbits)	49	40.6	31.6	195	145
M9Ks	38	31	15	38	31
Multipliers (18-bits)	24	33	33	24	33
Fmax (data rate,MHz)	375	533	566	376	533
SQNR	87.8	86.7	86.7	81.3	82.9
µJ/FFT	1.29	1.12		6.36	4.31

In the table above the adaptive logic module (ALM) is the basic unit of a Stratix III FPGA (one 8-input LUT, two registers plus other logic). Comparison with Xilinx Virtex 5 devices can be made by noting that two M9K memories are equivalent to a Xilinx BRAM and that an ALM is equivalent to between 1.2 and 1.8 LEs, since benchmark studies show 1 ALM=1.2 LEs (Xilinx white paper WP284 v1.0, December 19, 2007) and 1 ALM=1.8 LEs (Intel white paper), respectively.

The memory size (Kbits) indicates the total used memory in the M9Ks and is a measure of how fully utilized they are. (Considerable memory savings are possible if streaming operation is not necessary and data can be provided in out-of-order sequence.) The 256-pt "v2" circuit uses "distributed memory" (MLABs in Intel FPGAs) insteady of the embedded memories, as sometimes this leads to more efficient resource usage.

Power estimates (microjoules/FFT) were obtained from the PowerPlay analyzer tool using value change dump (vcd) files from Modelsim simulations to obtain accurate toggle rates.

Operation at 500MHz has been verified using an Intel Stratix III development kit, which included an EP3SL150F1152C2 FPGA. (The Fmax values were based on the best of ~20 seeds for each circuit).

Device Family Support

Intel Device Families Supported

- Stratix
- Aria
- Cyclone
- Hardcopy

Xilinx Device Families Supported

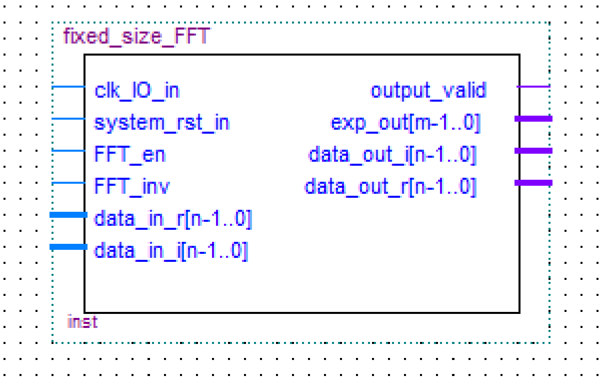
- Virtex 4-7
- Spartan
- Artix-7

Deliverables

- Netlist (e.g., for Intel FPGAs a *.qxp file for synthesis or a *.vo file for simulation)
- Synthesis constraints (e.g., for Intel FPGA’s an *.sdc file)
- Modelsim Testbench (*.vo file for DFT circuit plus verilog testbench for control). Matlab verification utilities also available.
- Intel Stratix III FPGA board development kit testbench
- Matlab behavioral bit-accurate model (p-code)
- Documentation

Pin-outs

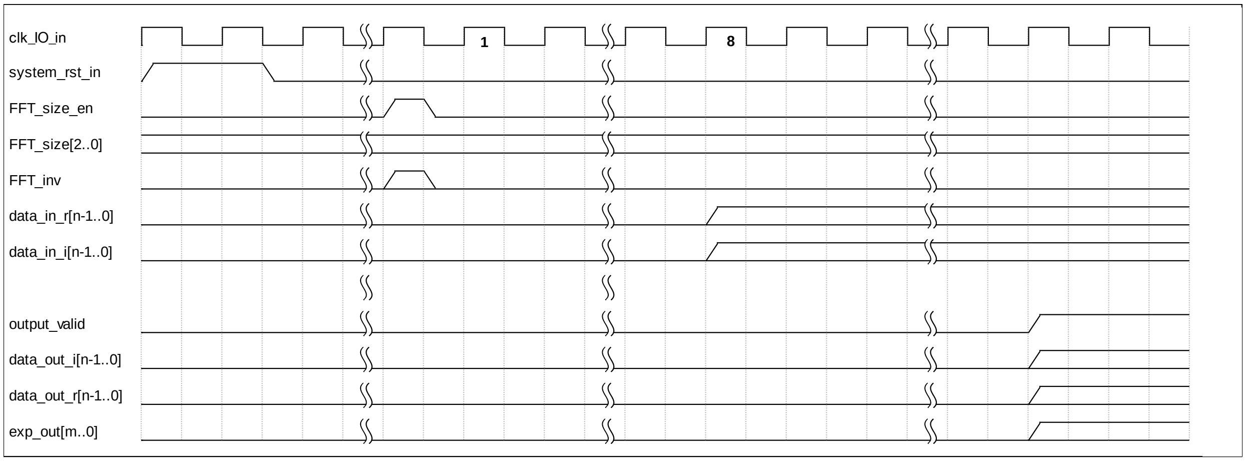
A symbol list corresponding to the pin-outs shown below are provided in the accompaning table. These apply to the "nominal variable" FFT circuit. Depending upon the desired interfaces, some signals could change.



Name	Signal	Description
clk_IO_in	clock	Can be either a low frequency board oscillator clock output in which case circuit clock is derived from a PLL or actual data I/O clock
system_rst_in	control	Resets circuit; active high
FFT_en	control	Registers FFT_inv signal; active high
FFT_inv	control	High->forward; low->inverse
data_in_r/i	n-bit signed	Real and imaginary inputs
output_valid	control	High during data output
exp_out	m-bit unsigned	Exponents (one per real/imag data pair)
data_out_r/i	n-bit signed	Real and imaginary outputs

Timing Diagram

A variety of timing possibilities exist depending upon the desired interface. That shown here is applicable to a streaming, normal order input/output scheme.



At any time after system_rst_in goes low, FFT_ en is used to latch the direction of the transform (FFT_inv=0/1 for forward/inverse). Following this, the circuit expects to see continuous data appearing on the 8th subsequent cycle. Valid data out occurs when output_valid goes high. For streaming operation output is continuous from this point on.